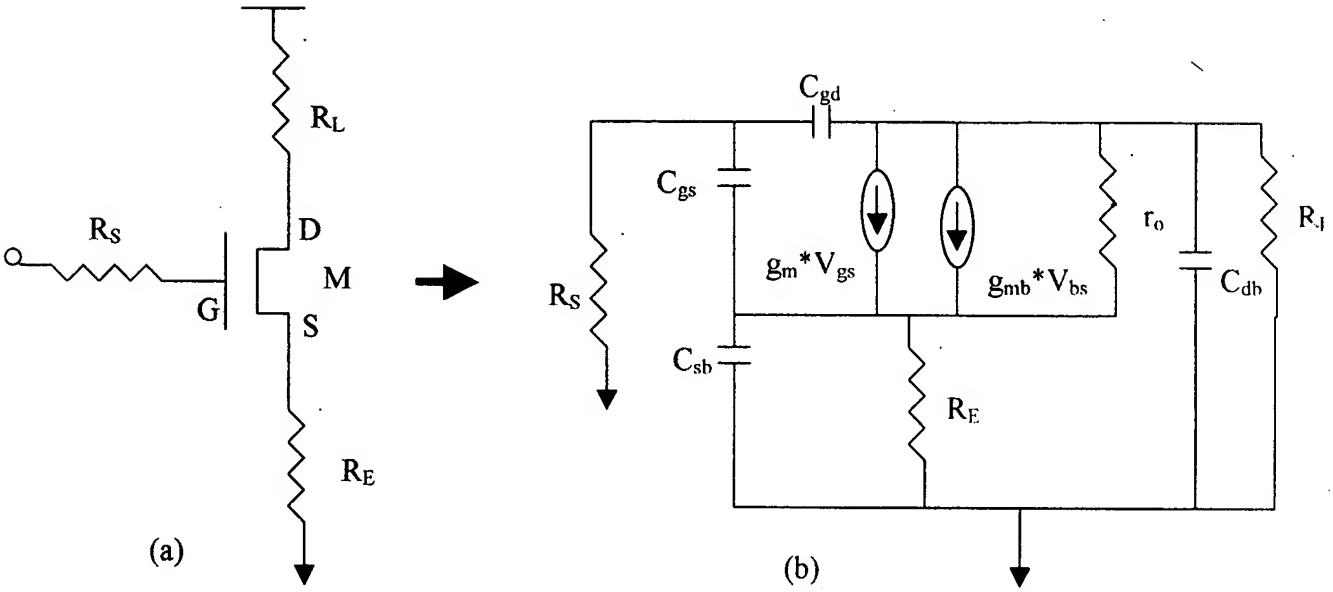
DRAWING

Fig. 1 -- Concept of Open Circuit Time Constant



Equivalent Resistive Impedance at Node G:

$$r_G = (R_S + R_E) / (1 + g_m * R_E)$$

Equivalent Resistive Facing C_{gs}:

$$r_{gs} = R_L + R_S + g_m / (1 + g_m * R_E)$$

Fig. 2 -- Parasitic Loading Constraints Generation Flow Chart

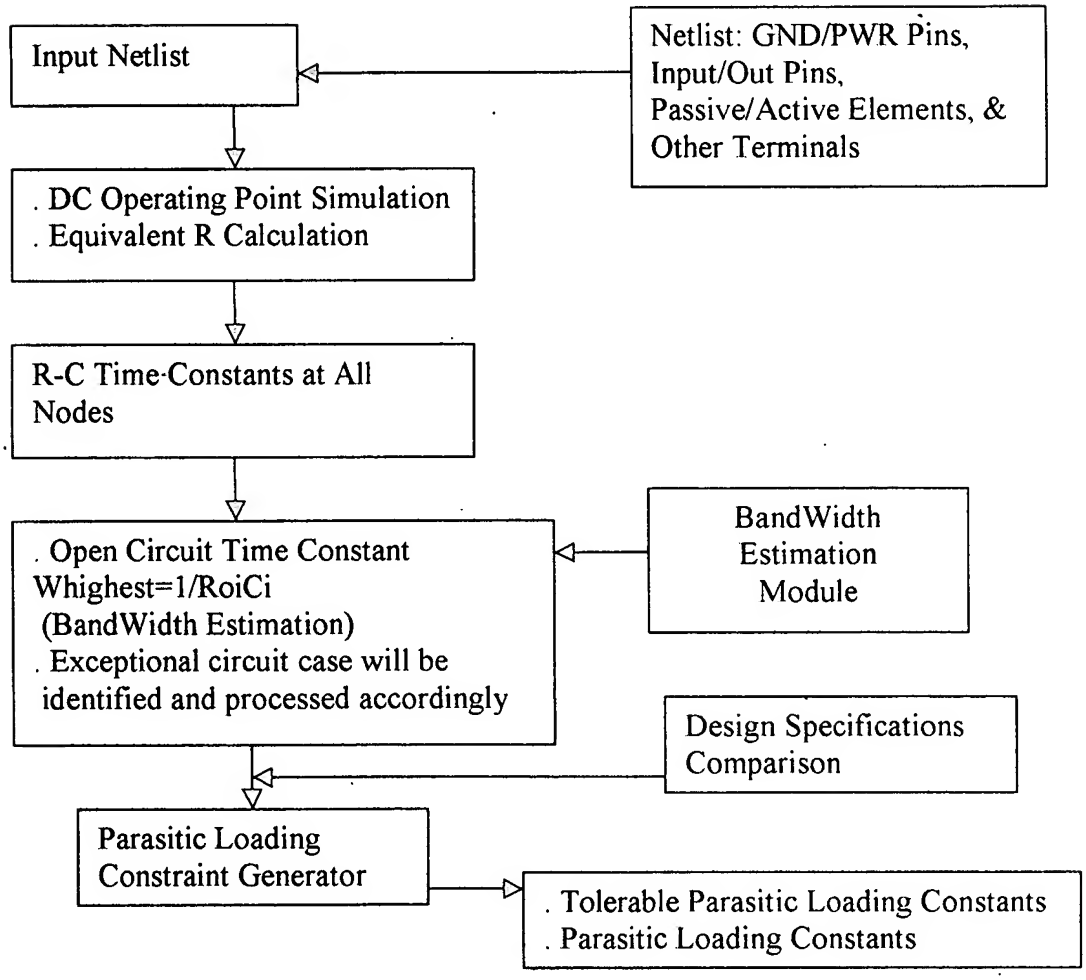


Fig. 3 -- Means of Circuit Physical Synthesis, Selecting Optimal Circuit Topology Parasitic Capacitance, Parasitic Inductance, and Routing Solution, and Means of Stability Analysis and Optimizing Circuit Performance Flow Chart